

**DESCRIPTION**

The LX5240 is a multimode SCSI terminator with plug-and-play capability that conforms to the SCSI Parallel Interconnect-2 (SPI-2) specification developed by the T10 standards committee for low voltage differential (LVD) termination, while providing backwards compatibility to the SCSI, SCSI-2, and SPI single-ended specifications. Multimode compatibility permits the use of legacy devices on the bus without hardware alterations. Automatic mode selection is achieved through voltage detection on the diffsense line.

The LX5240 utilizes Linfinit's UltraMAX technology which delivers the ultimate in SCSI bus performance while saving component cost and board area. Elimination of the external capacitors also mitigates the need for a lengthy capacitor selection process. The individual high bandwidth drivers also maximize channel separation and reduce channel to channel noise and cross talk. The high bandwidth architecture insures ULTRA2 performance while providing a clear migration path to ULTRA3 and beyond.

When the LX5240 is enabled, the differential sense (DIFFSENSE) pin supplies a voltage between 1.2V and 1.4V. In application, this pin

is tied to the DIFFSENSE input of the corresponding LVD transceivers. This action enables the LVD transceiver function. DIFFSENSE is capable of supplying a maximum of 15mA. Tying the DIFFSENSE pin high places the LX5240 in a HI Z state indicating the presence of an HVD device. Tying the pin low places the part in a single-ended mode while also signaling the multimode transceiver to operate in a single-ended mode.

The LX5240 supports full Plug and Play functionality with the DISCONNECT A and B pins. These logic compatible pins place the device in operational or sleep modes. During sleep mode, power dissipation is reduced to a meager 15µA while also placing all outputs in a HI Z state. Also during sleep mode, the DIFFSENSE function is disabled and is placed in a HI Z state.

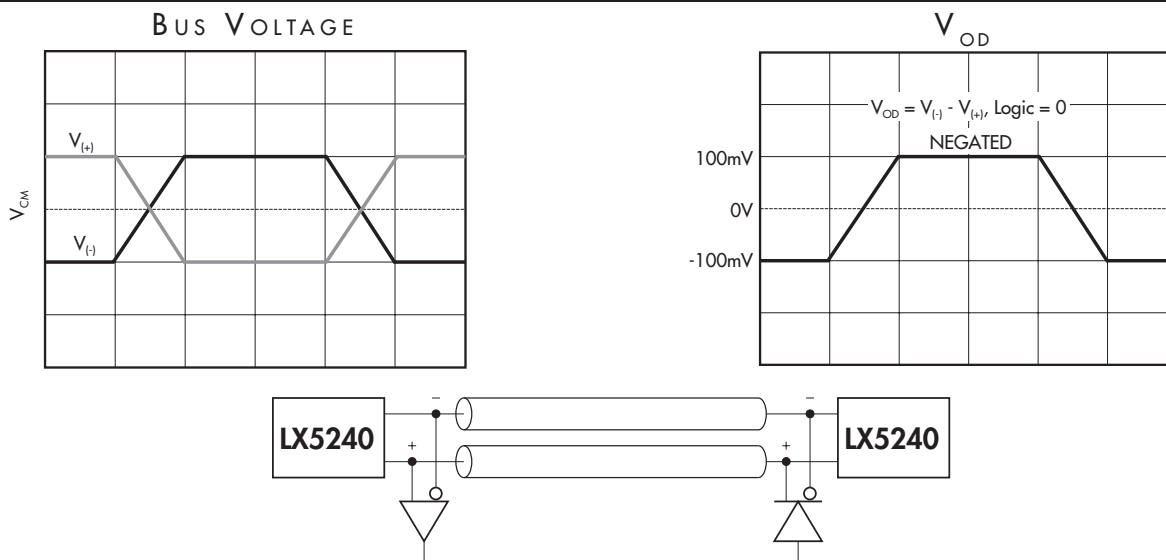
Another key feature of the LX5240 is the master / slave function. Driving this pin high or floating the pin enables the 1.3V DIFFSENSE reference. Driving the pin low disables the on board DIFFSENSE reference and enables use of an external master reference device.

**KEY FEATURES**

- Auto-Selectable LVD Or Single-Ended Termination
- 3.0pF Maximum Disabled Output Capacitance
- Fast Response, No External Capacitors Required
- Compatible With Active Negation Drivers
- 15µA Supply Current In Disconnect Mode
- Logic Command Disconnects All Termination Lines
- Diffsense Line Driver
- Ground Driver Integrated For Single-Ended Operation
- Current Limit And Thermal Protection
- Hot-Swap Compatible (Single-Ended)
- Compatible With SCSI 1, 2, 3, Fast-20, And The Pending SPI-2 LVD
- Plug And Play Compatible
- See LX5245/5246, LVD Termination Only

**NOTE:** For current data & package dimensions, visit our web site: <http://www.linfinit.com>.

**PRODUCT HIGHLIGHT**



**PACKAGE ORDER INFO**

$T_A$ (°C)	<b>DB</b> Plastic SSOP 36-pin	<b>PW</b> Plastic TSSOP 24-pin
0 to 70	LX5240CDB	LX5240CPW

Note: All surface-mount packages are available in Tape & Reel. Append the letter "T" to part number. (i.e. LX5240CDBT)

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#### ABSOLUTE MAXIMUM RATINGS (Note 1)

TermPwr Voltage .....	+7V
Operating Junction Temperature	
Plastic (DB, PW Packages) .....	150°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 seconds) .....	300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

#### THERMAL DATA

##### DB PACKAGE:

**THERMAL RESISTANCE-JUNCTION TO AMBIENT,  $\theta_{JA}$**       **50°C/W**

##### PW PACKAGE:

**THERMAL RESISTANCE-JUNCTION TO AMBIENT,  $\theta_{JA}$**       **100°C/W**

Junction Temperature Calculation:  $T_j = T_A + (P_D \times \theta_{JA})$ .

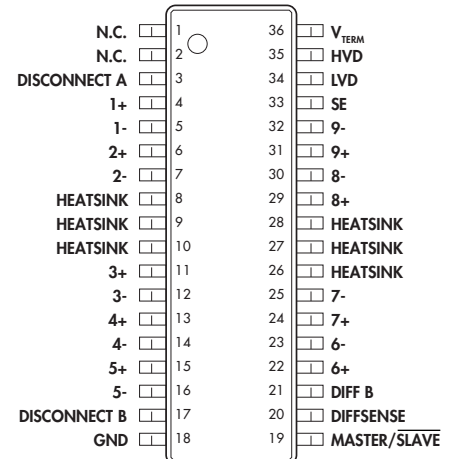
The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

MASTER / SLAVE FUNCTION TABLE

MASTER / SLAVE	DIFFSENSE Status	Output Current
L*	HI Z	0mA
H	1.3V	15mA Source
Open (Pull-up)	1.3V	15mA Source

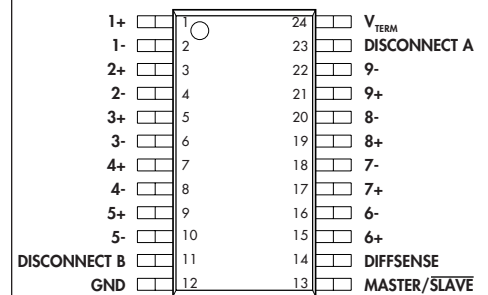
\* When in Low state, terminator will detect state of DIFFSENSE line.

#### PACKAGE PIN OUTS



##### DB PACKAGE (Top View)

("N.C." = No Internal Connection)



##### PW PACKAGE (Top View)

("N.C." = No Internal Connection)

DIFFSENSE / POWER UP / POWER DOWN FUNCTION TABLE

DISCONNECT A	DISCONNECT B	DIFF SENSE	Outputs		Quiescent Current
			Status	Type	
H L	L H	L < 0.5V	Enable	S.E.	7mA
H L	L H	0.7 to 1.9V	Enable	LVD	21mA
H L	L H	H > 2.4V	Disable	HI Z	1mA
L H Open	L H Open	X	Disable	HI Z	10µA

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## RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Tempwr Voltage	LVD	3.0		5.25	V
	SE	3.5		5.25	V
Signal Line Voltage		0		5.0	V
Disconnect Input Voltage		0		$V_{TERM}$	V
Operating Virtual Junction Temperature Range					
LX5240C		0		70	°C

Note 2. Range over which the device is functional.

## ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperature range of  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ . TermPwr = 4.75V, DISCONNECT A or B = L. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Symbol	Test Conditions	LX5240			Units
			Min.	Typ.	Max.	
<b>LVD Terminator Section</b>						
TermPwr Supply Current	LVD $I_{CC}$	All term lines = Open		25	30	mA
		DISCONNECT A or B = LOW		15	35	$\mu\text{A}$
Common Mode Voltage	$V_{CM}$		1.125	1.25	1.375	V
Offset Voltage	$V_{FSB}$	Open circuit between - and + (see Note 3)	100	112	125	mV
Differential Terminator Impedance	$Z_D$	$V_{OUT}$ Differential = -1V to 1V	100	105	110	$\Omega$
Common Mode Impedance	$Z_{CM}$	0V to 2.5V	100	200	300	$\Omega$
Output Capacitance	$C_O$	DISCONNECT A or B = LOW		2.5		pF
Output Leakage	$I_{LEAK}$	DISCONNECT A or B = LOW, $V_{LINE} = 0$ to 4V, $T_A = 25^{\circ}\text{C}$			2	$\mu\text{A}$
		DISCONNECT A or B = LOW, $V_{TERM} = 0\text{V}$ , $V_{LINE} = 2.7\text{V}$		1		$\mu\text{A}$
Mode Change Delay	$t_{DF}$	DIFFSENSE = 1.4V to 0V		115		ms
<b>DIFFSENSE Section</b>						
DIFFSENSE Output Voltage	$V_{DIFF}$		1.2	1.3	1.4	V
DIFFSENSE Output Source Current	$I_{DIFF}$	$V_{DIFF} = 0\text{V}$	5.0		15.0	mA
DIFFSENSE Sink Current	$I_{SINK(DIFF)}$	$V_{DIFF} = 2.75\text{V}$			200	$\mu\text{A}$
DIFFSENSE Output Leakage	$I_{LEAK(DIFF)}$	DISCONNECT A or B = LOW, $T_A = 25^{\circ}\text{C}$			10	$\mu\text{A}$
<b>Single-Ended Termination Section</b>						
Tempwr Supply Current	SE $I_{CC}$	All term lines = Open, Master/Slave = 0V		7	10	mA
		All term lines = 0.2V, Master/Slave = 0V		214	226	mA
		DISCONNECT A or B = LOW		15	35	$\mu\text{A}$
Terminator Output High Volt	$V_O$		2.6	2.85		V
Output Current	$I_O$	$V_{OUT} = 0.2\text{V}$	21	23	24	mA
Sink Current	$I_{SINK}$	$V_{OUT} = 4\text{V}$ , All lines	45	65		mA
Output Capacitance	$C_O$	DISCONNECT A or B = LOW		2.5		pF
Leakage Current	$I_{LEAK}$	DISCONNECT A or B = LOW, $V_{OUT} = 0$ to 4V, $T_A = 25^{\circ}\text{C}$			2	$\mu\text{A}$
		DISCONNECT A or B = LOW, $V_{TERM} = 0\text{V}$ , $V_{LINE} = 2.7\text{V}$		1		$\mu\text{A}$
Ground Driver Impedance	$Z_G$	$I = 1\text{mA}$			100	$\Omega$
Thermal Shutdown				150		°C

Note 3. Open circuit failsafe voltage.

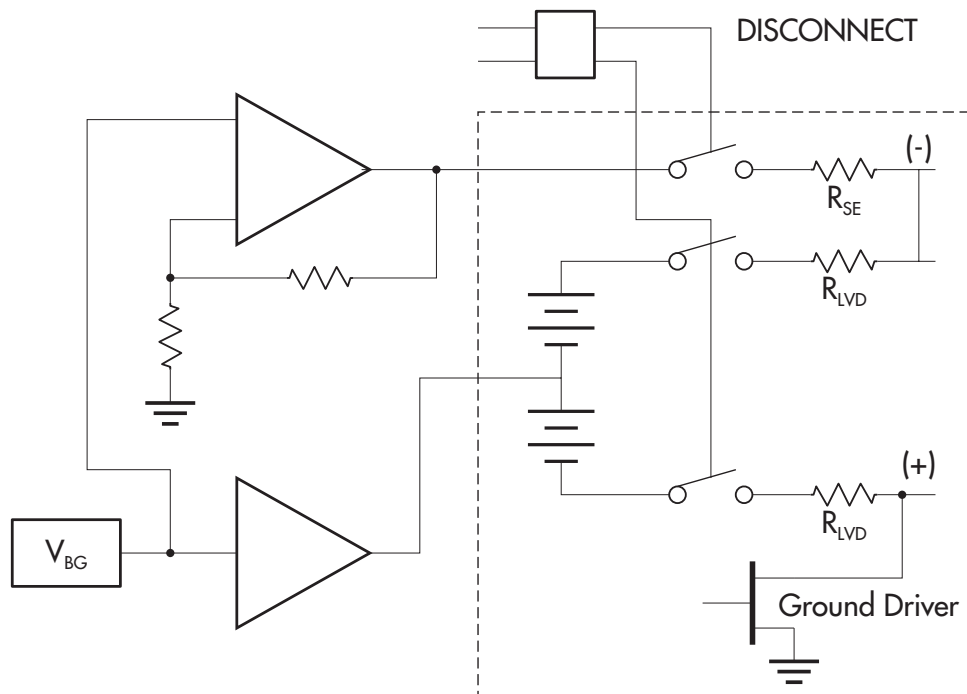
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**ELECTRICAL CHARACTERISTICS**

Parameter	Symbol	Test Conditions	LX5240			Units
			Min.	Typ.	Max.	
<b>DISCONNECT Section</b> (Plug n' Play)						
DISCONNECT A/B Thresholds	$V_{TH}$		0.8		2.0	V
Input Current	$I_{IL}$	DISCONNECT A/B = 0V			10	$\mu A$
	$I_{IH}$	DISCONNECT A/B = 2.4V		100		nA
<b>MASTER / SLAVE Section</b>						
MASTER / SLAVE Thresholds	$V_{TH(MS)}$		0.8		2.0	V
Input Current	$I_{IL(MS)}$	MASTER / SLAVE = 0V			10	$\mu A$
	$I_{IH(MS)}$	MASTER / SLAVE = 2.4V		100		nA

**BLOCK DIAGRAM**

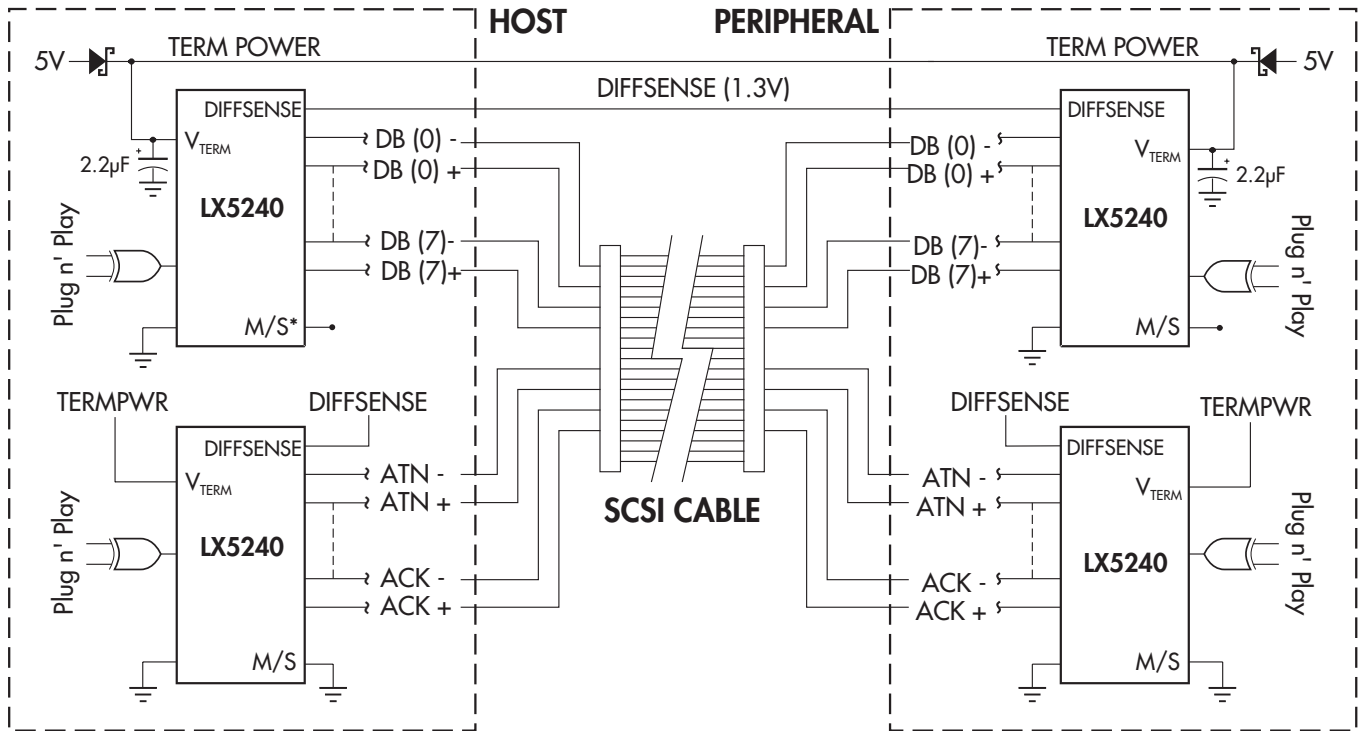


**FIGURE 1** — LX5240 Block Diagram

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APPLICATION SCHEMATIC



Note: Single-ended the + signals become ground, DIFFSENSE < 0.5V.

\* M/S = MASTER/S�AVE

FIGURE 2 — LX5240 Application Schematic

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